

**HANDS ON TRAINING WITH C A D E N C E
FOR MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN**



IC DESIGN & FABRICATION CENTRE
Department of Electronics & Telecommunication Engineering
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[1] VLSI Design using EDA Tools & Cadence

- a) Introduction to EDA Tools
- b) Basic gates design using Schematic Capture
- c) Netlisting Using T-Spice
- d) Verification of design using waveform editor
- e) Circuit Optimization
- f) Introduction to Cadence
- g) Design and Optimization of different digital circuits.
- h) Design of basic analog ckts. and diff. analyses using Virtuso.
- i) Layout Designing using Virtuso-XL
- j) Post layout simulation

[2] Fabrication and Characterization of semiconductor devices

- a) Mask Fabrication by auto cad
- b) Theoretical Simulation by supreme 2
- c) Hardware fabrication for all process of Microelectronics: cleaning, etching, oxidation, diffusion, photolithography and Metallization.
- d) Characterization of fabricated device.
- e) Theoretical Simulation by Coventor Ware
- f) Hardware Fabrication by MEMS

Duration: 6 months [Course starts from 1st week of November 2011 tentatively. Final date will be announced later on]

Time: 11.00 AM to 4.00 PM [Two days per week]

Eligibility: The Candidate should be at least B.E./B.Tech 3rd year and above in Electronics and Communication / Instrumentation / Electrical / Computer Science / Information Technology.

Admission: Application on Plain Paper and address to 'The Co-ordinator, IC Design & Fabrication Centre, Department of Electronics & Telecommunication Engineering Department, Jadavpur University, Kolkata - 700032. Last date of submission 24th October 2011.

Fees: @ Rupees **20,000/-** in demand draft should be drawn in favour of "**REGISTRAR, JADAVPUR UNIVERSITY**", payable at Kolkata.

Total Seat: 12 Per batch

Enclosure: One copy of PS Photograph, **Xerox copy** of Madhyamik Admit Card, HS Marksheet, all Semesters Marksheet & other certificates. [Attested copies of Marksheets/Certificates to be enclosed]